a second interconnect metal located on or in a second interlevel dielectric layer, the second interlevel dielectric layer located over the first interlevel dielectric layer;

a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over the second dielectric layer; and

a via located through the second and third interlevel dielectric layers and connecting the first and third interconnect metals, the via being void of a landing pad between the second and third interlevel dielectric layers.

(2) Please add the following new Claims 29-30 as follows:

–29. (New) A semiconductor device, comprising:

a first metal feature located on a semiconductor surface;

a first etch stop layer located on the first metal feature;

a first interlevel dielectric layer located on the first etch stop layer;

a second etch stop layer located on the first interlevel dielectric layer;

a second interlevel dielectric layer located on the second etch stop layer;

an unsegmented via located through the first and second etch stop layers and interlevel dielectric layers, the unsegmented via extending to and contacting the first metal feature and being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer; and